Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (currently amended) An integrated circuit package, comprising:

a die attach pad having a first and second surface, the first and second surface being on opposite sides of the die attach pad;

an integrated circuit die mounted on the first surface, the integrated circuit die having a plurality of terminal pads; and

a substrate, the substrate comprised of a dummy layer, a dielectric layer, and a solder mask structure, which encapsulates the dummy layer and the dielectric layer, the substrate mounted on the first surface, the substrate having an aperture where the aperture encompasses the integrated circuit die, and the substrate having [[one or more conductive]] and separating a plurality of conduction bands.

2. (original) The package of claim 1 further including a heat sink where the second surface of the die attach pad is adjacent to the heat sink.

3. (original) The package of claim 2 where the heat sink comprises one or more disk shaped portions.

4. (original) The package of claim 3 where the heat sink comprises two disk shaped portions having a first disk shaped

portion adjacent to the die attach pad and a second disk shaped portion adjacent to the first disk shaped portion, the first disk shaped portion having a diameter that is greater than the second disk shaped portion.

5. (original) The package of claim 2 where the heat sink comprises aluminum or copper coated with nickel.

6. (currently amended) The package of claim 1 where the [[substrate comprises a]] plurality of [[conductive]] conduction bands are located between the inner edge forming the aperture and the outer edge of the substrate.

7. (currently amended) The package of claim 1 where the [[one or more]] plurality of conduction bands are ground planes or power planes.

8. (currently amended) The package of claim 1 where the substrate is substantially rectangular with a substantially rectangular aperture [[having a plurality of conduction bands along each of the four edges of the substrate]].

9. (cancelled)

10. (original) The package of claim 1 wherein the integrated circuit die is mounted on the die attach pad using a thermally conductive, electrically insulating adhesive.

11. (original) The package of claim 2 where the heat sink is attached to the die attach pad using a thermally conductive epoxy.

12. (original) The package of claim 1 where the substrate is mounted on the die attach pad using a thermally conductive epoxy or an adhesive tape.

13. (currently amended) The package of claim 1 wherein the [[one or more]] plurality of conduction bands are connected to internal lead fingers using wire bonds.

14. (currently amended) The package of claim 13 wherein the wire bonds are formed using copper wires coated with silver or gold.

15. (canceled)

16. (original) The package of claim 1 wherein the die attach pad further includes tie-bar extensions.

17. (original) The package of claim 1 wherein the integrated circuit die is an ASIC, FPGA, or a CPLD.

18. (currently amended) A method of packaging an integrated circuit comprising:

attaching an integrated circuit die on a die attach pad, the die attach pad having a first and second surface, the first and second surface being on opposite sides of the die

attach pad, wherein the integrated circuit die is mounted on the first surface of the die attach pad;

mounting a substrate on the first surface of the die attach pad, the substrate having an aperture where the aperture encompasses the integrated circuit die, the substrate having [[one or more conductive]] and separating a plurality of conduction bands [[between the outer edge of the substrate and the inner edge forming the aperture]], and the substrate comprising a dummy layer, a dielectric layer, and a solder mask structure, which encapsulates the dummy layer and the dielectric layer.

19. (original) The method of claim 18 further including placing a heat sink adjacent the second surface of the die attach pad.

20. (currently amended) The method of claim 19 where the placing [[comprising]] comprises attaching the heat sink to the die attach pad using an epoxy or a tape adhesive.

21. (original) A data processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

an integrated circuit die package of claim 1.

22. (original) A printed circuit board on which is mounted an integrated circuit package of claim 1.

23. (original) The printed circuit board of claim 22 further comprising a processing circuitry coupled to the integrated circuit package.

24. (original) The printed circuit board of claim 23 further comprising a memory coupled to the processing circuitry and to the integrated circuit package.

25. (currently amended) An integrated circuit package, comprising:

a die attach pad means having a first and second surface, the first and second surface being on opposite sides of the die attach pad means;

an integrated circuit die means mounted on the first surface, the integrated circuit die means having a plurality of terminal pads; and

a substrate means mounted on the first surface, the substrate means having an aperture where the aperture encompasses the integrated circuit die means, the substrate means having [[one or more conductive]] and separating a plurality of conduction means, and the substrate means comprising a dummy layer, a dielectric layer, and a solder mask structure, which encapsulates the dummy layer and the dielectric layer.